Dkt: 1376.718US1

Page 2

Serial Number: 10/643,769 Filing Date: August 18, 2003

Title: SCHEDULING SYNCHRONIZATION OF PROGRAMS RUNNING AS STREAMS ON MULTIPLE PROCESSORS

IN THE SPECIFICATION

Please amend the paragraph beginning on page 1 at line 10, as follows:

This application is related to U.S. Patent Application No, entitled
"SCHEDULING SYNCHRONIZATION OF PROGRAMS RUNNING AS STREAMS ON
MULTIPLE PROCESSORS", filed on even date herewith; U.S. Patent Application No.
[[]] 10/643,744, cntitled "Multistream Processing System and Method
Multistreamed Processor Vector Packing Method and Apparatus", filed on even date herewith; to
U.S. Patent Application No. [[]] 10/643,577, entitled "System and Method
for Synchronizing Memory Transfers Processing Memory Instructions", Serial No.
[[]], filed on even date herewith; to U.S. Patent Application No.
[[]] 10/643,742, entitled "Decoupled Store Address and Data in a
Multiprocessor System", filed on even date herewith; to U.S. Patent Application No.
[[]] 10/643,586, entitled "Decoupled Vector Scalar/Vector Computer
Architecture System and Method (as amended)", filed on even date herewith; to U.S. Patent
Application No. [[]] 10/643,585, entitled "Latency Tolerant Distributed
Shared Memory Multiprocessor Computer", filed on even date herewith; to U.S. Patent
Application No. [[]] 110/643,754, entitled "Relaxed Memory Consistency
Model", filed on even date herewith; to U.S. Patent Application No. [[]] 10/643,758,
entitled "Remote Translation Mechanism for a Multinode System", filed on even date herewith;
and to U.S. Patent Application No.[[]] 10/643,741, entitled "Method and
Apparatus for Local Synchronizations in a Vector Processor System Multistream Processing
Memory-And Barrier-Synchronization Method and Apparatus", filed on even date herewith,
each of which is incorporated herein by reference.

Please amend the paragraph beginning on page 8 at line 7, as follows:

During the execution of one or more of the threads and/or streams within the thread, a context shifting event may occur (block 340). There are multiple reasons for context shift events, the quantity and type of context shifting event will depend on the operating environment. Typically the context shift will require [[that]] an elevated privilege for the thread or stream. In some embodiments, the elevated privilege is achieved by entering kernel mode.

Please amend the paragraph beginning on page 9 at line 10, as follows:

The stream that enters kernel mode will typically be executing using a kernel stack. As the stream is executing in kernel mode, it may or may <u>not</u> need to block within the kernel to wait for the availability of a resource (block 342). If the stream does not need to block within the kernel, the other streams executing on other processors of multiple processor unit 102 continue to operate in user (non-privileged) mode (block 350). An example of a case where a stream entering the kernel may not need to block is when the stream needs to interact with a TLB (Translation Lookaside Buffer). Typically the code executed in the kernel for this type of operation is fairly short, and does not have the potential for interfering with other streams or processes.